Patent Claims

1. A semiconductor component having a light-emitting semiconductor layer or a light-emitting semiconductor element (2) and two contact locations (3, 8), which are formed as a contact layer (3) and a contact (8), characterized
in that the component is arranged on a carrier substrate (7) and the carrier substrate (7) is patterned vertically or horizontally.

2. The semiconductor component as claimed in claim 1, in which the carrier substrate (7) has a carrier base (24) that is spatially separated from the semiconductor layer (2) at least by an interspace (26) and a vertical structure element (25).

3. The semiconductor component as claimed in claim 1 or 2,
in which the carrier substrate (7) is formed in one piece.

4. The semiconductor component as claimed in claims 1 to 3,
in which at least one structure element (25) is situated centrally above the center of the semiconductor layer (2).

5. The semiconductor component as claimed in one of claims 1 to 4,
in which the structure element (25) is circular or rectangular in cross section.

6. The semiconductor component as claimed in one of claims 1 to 5,
in which the structure element or the structure elements has/have an aspect ratio of at least two.

7. The semiconductor component as claimed in one of claims 1 to 6,
in which the ratio of semiconductor layer length/structure element height does not exceed 15.

8. The semiconductor component as claimed in one of claims 1 to 7,
in which the interspaces (26) are filled with a filling material (27) that is more elastic than the material of the carrier substrate (7).

9. The semiconductor component as claimed in claim 1,
in which the carrier substrate (7) comprises an electrically conductive layer sequence, the layers of which are coordinated with one another in terms of thickness such that no or hardly any bending moment arises in the layer assembly including the semiconductor layer (2), the layer having the smallest expansion coefficient (20) being arranged the furthest away from the semiconductor layer (2).

10. The semiconductor component as claimed in one of claims 1 to 9,
in which at least one wetting layer (6) is formed between the carrier substrate (7) and the contact location (3) situated nearer to the carrier substrate (7).

11. The semiconductor component as claimed in one of claims 1 to 10,
in which at least one reflection layer (4) is arranged between the contact location (3) and the carrier substrate (7) or between the contact location (3) and the wetting layer (6).

12. The semiconductor component as claimed in one of claims 1 to 11,
in which at least one diffusion barrier (5) is arranged

between the reflection layer (4) and the carrier substrate (7) or between the reflection layer (4) and the wetting layer (6).

13. The semiconductor component as claimed in one of claims 1 to 12,
in which the carrier substrate (7) is electrically conductive.

14. A method for producing a light-emitting semiconductor component, which has the following method steps:

(a) epitaxial deposition of a light-emitting semiconductor layer (2) on a growth substrate (1),

(b) provision of the semiconductor layer (2) with a metallic contact layer (3),

(c) production of an adhesion and wetting layer (6) at least above the metallic contact layer (3),

(d) application, production or deposition of a mechanically stable carrier substrate (7) onto the adhesion and wetting layer (6),

(e) separation of the semiconductor layer (2) from the growth substrate (1),

(f) etching of mesa trenches (10) for the definition of individual chips between the mesa trenches (10), the mesa trenches (10) at least extending through the entire semiconductor layer (2) and the entire contact layer (3),

(g) application of an electrical contact (8) on the semiconductor layer (2), and

(h) singulation of the chips by separation along the mesa trenches (10).

15. A method for producing a light-emitting semiconductor component, which has the following method steps:

(a) epitaxial deposition of a light-emitting semiconductor layer (2) on a growth substrate (1),

(b) provision of the semiconductor layer (2) with a metallic contact layer (3),

(ba) etching of mesa trenches (10) for the definition of individual chips between the mesa trenches (10), the mesa trenches (10) at least extending through the entire semiconductor layer (2) and the entire contact layer (3),

(c) production of an adhesion and wetting layer (6) at least above the metallic contact layer (3),

(d) application, production or deposition of a mechanically stable carrier substrate (7) onto the adhesion and wetting layer (6),

(e) separation of the semiconductor layer (2) from the growth substrate (1),

(g) application of an electrical contact (8) on the semiconductor layer (2), and

(h) singulation of the chips by separation along the mesa trenches (10).

16. The method as claimed in claim 14 or 15, in which, after method step (b) a reflection layer (4) is applied on the contact layer (3) or integrated in

the contact layer (3).

17. The method as claimed in claim 16, in which a diffusion barrier (5) is applied on the reflection layer (4).

18. The method as claimed in one of claims 14 to 17, in which the contact layer in accordance with method step (b), the reflection layer (4), the barrier layer (5), the wetting layer (6) in accordance with method step (c) and/or the contact (8) in accordance with method step (g) are applied by means of sputtering or vapor deposition.

19. The method as claimed in one of claims 14 to 18, in which

- a selectively dissoluble material is used for the growth substrate (1), and
- the separation of the semiconductor layer (2) from the growth substrate (1) in accordance with method step (e) is effected by selective etching of the growth substrate (1).

20. The method as claimed in one of claims 14 to 19, in which

- prior to method step (a), a sacrificial layer comprising a selectively dissoluble material is applied to the growth substrate, so that method step (a) takes place on said sacrificial layer, and
- the separation of the semiconductor layer (2) from the growth substrate (1) in accordance with method step (e) is effected by selective etching of the sacrificial layer.

21. The method as claimed in one of claims 14 to 19, in which an already laminated substrate is used as the growth substrate (1), the laminated substrate having an adhesion layer with suitable desired breaking locations

at which the growth substrate (1) is separated from the semiconductor layer (2) in a targeted manner during method step (e).

22. The method as claimed in one of claims 14 to 19, in which the separation of the semiconductor layer (2) from the growth substrate (1) in accordance with method step (e) is effected by means of a laser lift-off method by using a laser to decompose the semiconductor layer (2) at the interface with the growth substrate (1).

23. The method as claimed in one of claims 14 to 22, in which the mechanically stable carrier substrate (7) is deposited by means of a sputtering method, a CVD method, a galvanic method or electroless plating.

24. The method as claimed in one of claims 14 to 23, in which, after method step (d), an additional auxiliary substrate (12) is applied to the carrier substrate (7).

25. The method as claimed in claim 24, in which the additional auxiliary substrate (12) is fixed onto the carrier substrate (7) by means of an adhesive-bonding method or soldering.

26. The method as claimed in claim 24 or 25, in which a solder layer (11) required for soldering and/or the auxiliary substrate (12) are/is applied by means of sputtering, vapor deposition or galvanically.

27. The method as claimed in one of claims 14 to 26, in which the carrier substrate (7) comprises a layer sequence, the layers of which are coordinated with one another in terms of thickness such that the layer having the largest modulus of elasticity (21) is the thinnest and the layer having the smallest modulus of

elasticity (20) is the thickest.

28. The method as claimed in one of claims 14 to 26, in which the total thickness of the carrier substrate (7) and, if appropriate, of the auxiliary substrate (12) and of the solder or adhesive-bonding layer (11) does not exceed 15 micrometers.

29. The method as claimed in one of claims 14 to 27, in which, after method step (g), a passivation layer (9) is applied at least partly over the semiconductor layer (2).

30. The method as claimed in one of claims 14 to 28, in which, after method step (g), three-dimensional structures for optimizing the coupling-out of light are applied to the semiconductor layer (2) and/or, if present, to the passivation layer (9).

31. The method as claimed in claim 30, in which the three-dimensional structures for optimizing the coupling-out of light are formed in pyramidal fashion with at least three visible areas per pyramid on the semiconductor layer (2) and/or the passivation layer (9) or in conical fashion on the semiconductor layer (2) and/or the passivation layer (9).

32. The method as claimed in claim 30 or 31, in which the three-dimensional structures for optimizing the coupling-out of light are produced by means of wet-chemical or dry etching.

33. The method as claimed in one of claims 15 to 32, in which, after method step b), a passivation layer (9) is applied at least partly over the semiconductor layer (2), the contact layer (3) and, if present, also over the reflection layer (4) and the diffusion barrier (5).

34. The method as claimed in one of claims 14 to 33, in which the chips are singulated by sawing or laser cutting in accordance with method step (h).

35. The method as claimed in one of claims 15 to 34, in which, after method step (c), separating ridges (13) are applied in the mesa trenches (10) on the wetting layer (6) in such a way that the separating ridges (13) completely fill the mesa trenches (10) over the entire length and project above the intervening surface of the wetting layer (6).

36. The method as claimed in claim 35, in which the separating ridges (13) are applied with a height of at least 10 micrometers above the trench bottom.

37. The method as claimed in one of claims 35 to 36, in which a photoresist is used as material for the separating ridges (13).

38. The method as claimed in one of claims 35 to 37, in which the separating ridges are applied by means of photolithography or the LIGA method.

39. The method as claimed in one of claims 35 to 38, in which the separating ridges (13) are formed in such a way that they have a tip in cross section.

40. The method as claimed in one of claims 35 to 39, in which method step (d) takes place only in the spaces between the separating ridges (13) and the carrier substrate material is applied up to the height of the separating ridges (13).

41. The method as claimed in one of claims 35 to 39, in which method step (d) takes place only in the spaces

between the separating ridges (13) and the carrier substrate material is applied beyond the height of the separating ridges (13).

42. The method as claimed in claim 41, in which, after method step (g), the material of the separating ridges (13) is selectively removed.

43. The method as claimed in claim 42, in which the material of the separating ridges (13) is dissolved by means of a solvent.

44. The method as claimed in one of claims 41 to 43, in which method step (h) is carried out by means of a shear process.

45. The method as claimed in one of claims 41 to 44, in which, during method step (h), the chips are singulated in strips (17) and are then mounted directly away from said strips (17) by means of a separating and bonding tool (18).

46. The method as claimed in claim 40, in which

- prior to method step (e), the material of the separating ridges (13) is selectively removed, carrier substrate islands (71) arising,
- the entire structure above the growth substrate (1) together with the projecting free carrier substrate islands (71) and mesa trenches (10) are then completely overformed by an auxiliary material (14), and
- the singulation is carried out in accordance with method step (h) by applying a carrier film (15) over the electrical contacts (8) on the semiconductor layer (2) and selectively removing the auxiliary material (14).

47. The method as claimed in claim 46,

in which a metal, polymer and/or glass-based material is used as the auxiliary material (14).

48. The method as claimed in one of claims 15 to 34, in which

- the application of the adhesion and wetting layer (6) in accordance with method step (c) is restricted only to the surface of the outermost layer,
- prior to method step (d), the mesa trenches (10) are completely covered with an anti-wetting layer (16),
- the application of the carrier substrate (7) in accordance with method step (d) accordingly takes place only onto the adhesion and wetting layer (6) and is stopped before adjacent carrier substrate islands (71) grow together,
- the entire structure above the growth substrate (1) together with the projecting free carrier substrate islands (71) and mesa trenches (10) are completely overformed by an auxiliary material (14), and
- the singulation is carried out in accordance with method step (h) by applying a carrier film (15) over the electrical contacts (8) on the semiconductor layer (2) and selectively removing the auxiliary material (14).

49. The method as claimed in one of claims 15 to 48, in which the production or the deposition of the carrier substrate (7) onto the adhesion and wetting layer (6) in accordance with method step (d) is carried out in the following manner:

- a photoresist is applied to the wetting layer (6) and patterned correspondingly throughout such that one or a plurality of negative forms of vertical structure elements (25) arise,
- the carrier substrate is applied into the negative forms and onto the photoresist until the formation of a carrier base (24) above the photoresist.

50. The method as claimed in claim 49,
in which the photoresist is selectively removed.

51. The method as claimed in claim 50,
in which the interspaces (26) resulting from removal of the photoresist are filled with a filling material (27).

52. The method as claimed in claim 51,
in which a filling material (27) more elastic than the material of the carrier substrate (7) is used.

53. The method as claimed in one of claims 49 to 52,
in which the photoresist is patterned in such a way that at least one negative form of a vertical structure element is provided below the center of the semiconductor layer (2).